CYF4455 Datasheet

PLL-based OOK/ASK Transmitter IC

1. GENERAL DESCRIPTION:

The CYF4455 is a high performance ASK/OOK transmitter for the Remote Keyless Entry (RKE) systems. It consists of a power amplifier, one-shot circuit and phase-locked loop with internal voltage controlled oscillator and loop filter. The one-shot circuit control the phase-locked loop and power amplifier to have fast start-up time in operation.

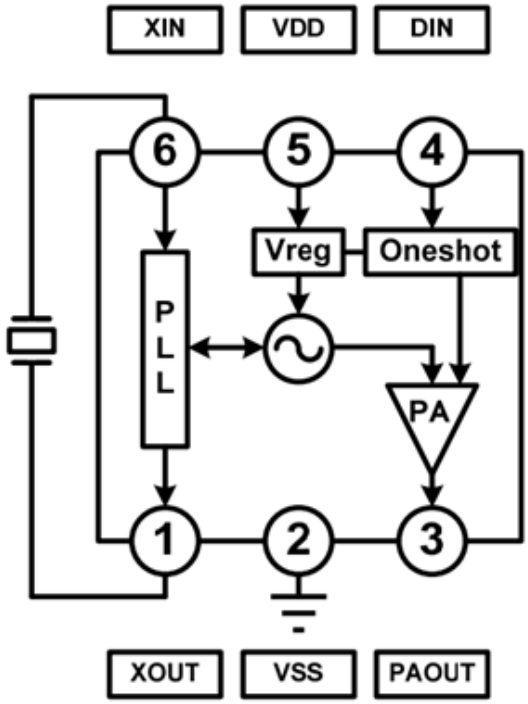
2. FEATURES:

- Highly integrated OOK/ASK transmitter
- High output power, 3 .3V /+14dBm / 12.5mA
- Low supply voltage, 2.2V to 3.6V operation range
- Low external component cost.
- PLL-based transmitter with frequency range from
- 250MHz to 450MHz
- On-chip one-shot circuit
- 60 dB RF on-off ratio for OOK/ASK modulation
- SOT23-6 package

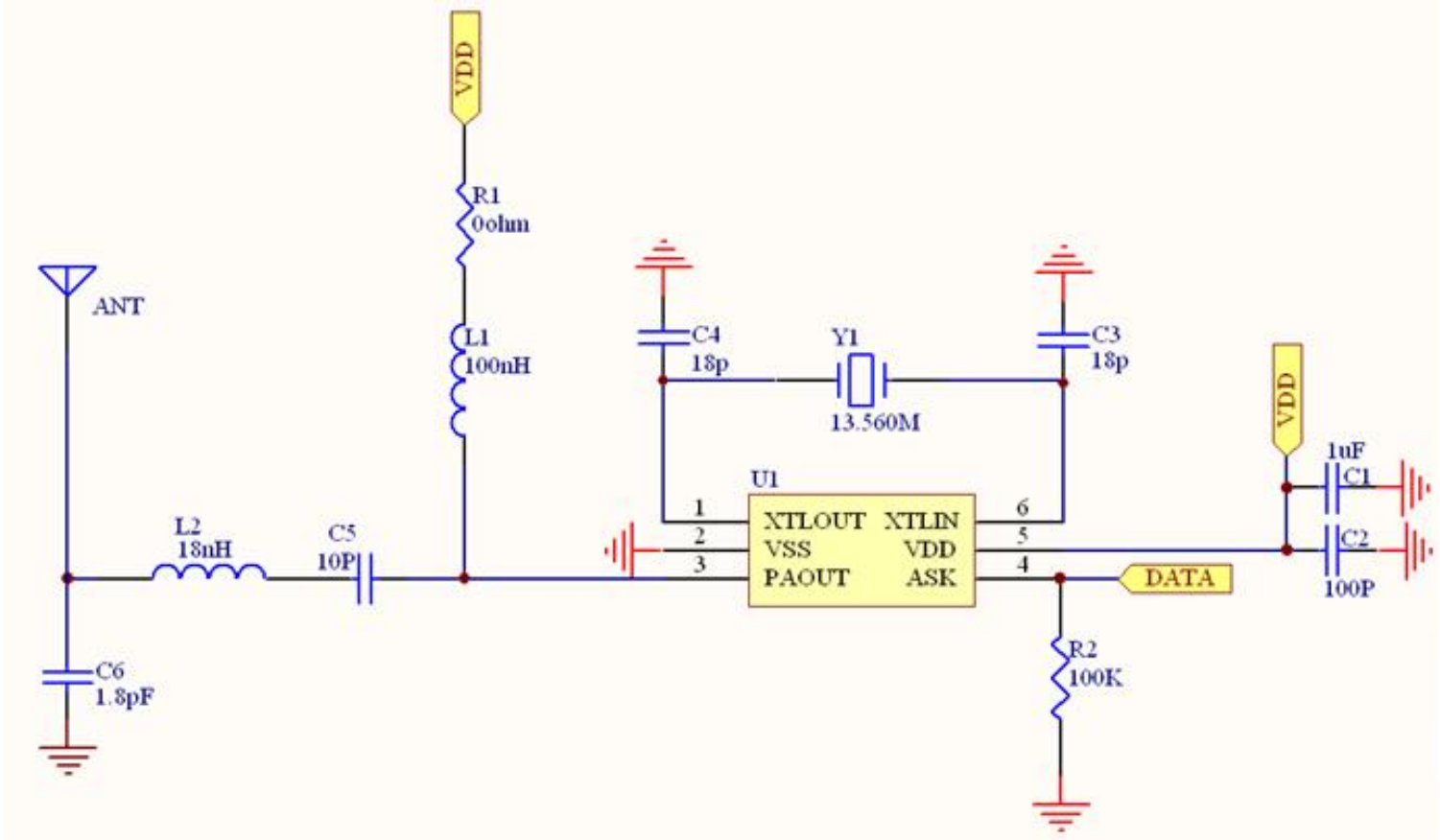
3. APPLICATIONS:

- Keyless entry systems
- Remote control systems
- Garage door openers
- Alarm systems
- Security systems
- Wireless sensors

4. BLOCK DIAGRAM:



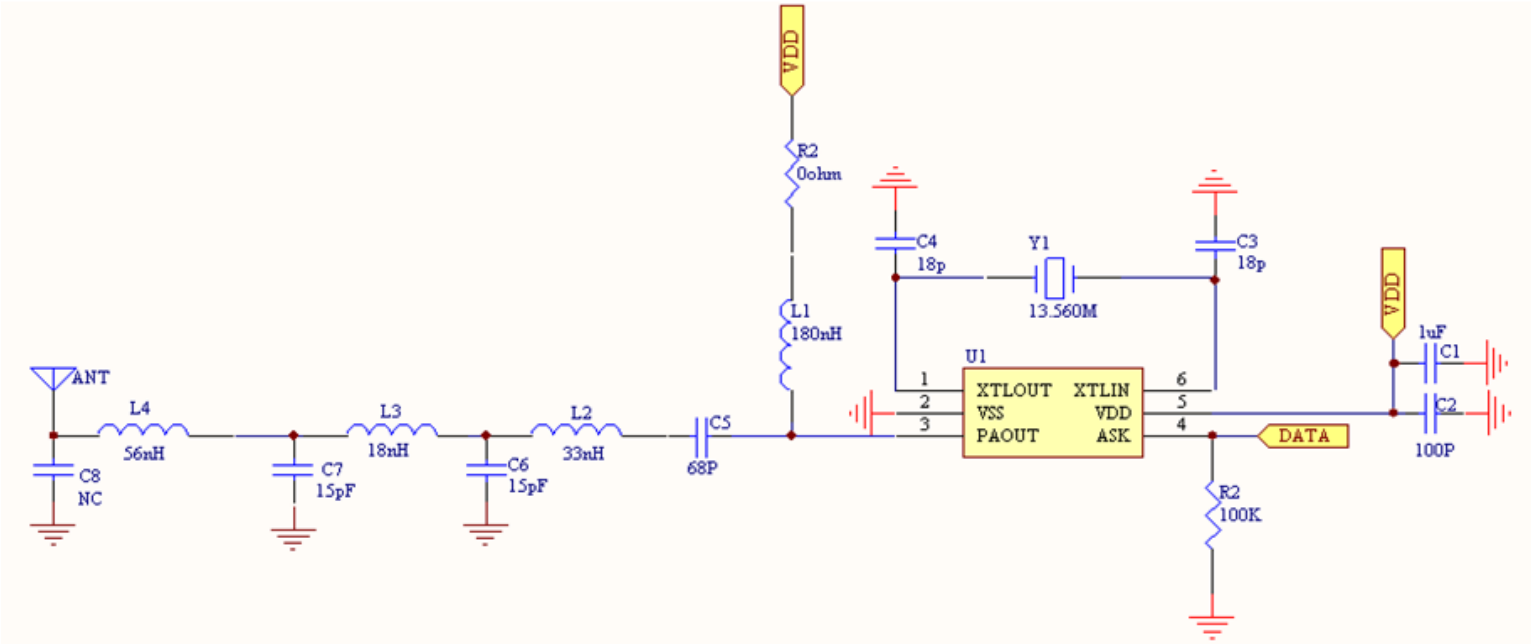
5. APPLICATION CIRCUIT:



BILL OF MATERIALS:

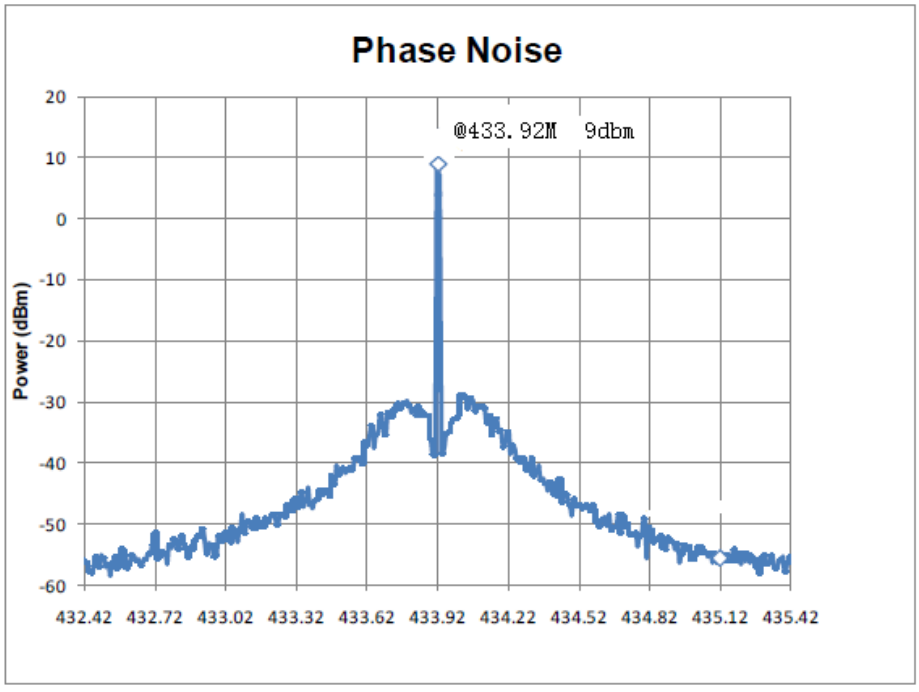
Part	Value		Unit
	315M	433.92M	
R1	100K	100K	Ω
R2	0	0	Ω
C1	1u	1u	F
C2	100p	100p	F
C3	18p	18p	F
C4	18p	18p	F
C5	10p	10p	F
C6	5.6p	1.8p	F
L1	100n	100n	H
L2	56n	18n	H
Y1	9.84375	13.560	Mhz
U1	CYF4455	CYF4455	

CERTIFIED CIRCUIT:



BILL OF MATERIALS:

Part	Value		Unit
	315M	433.92M	
R1	100K	100K	Ω
R2	0	0	Ω
C1	1u	1u	F
C2	100p	100p	F
C3	18p	18p	F
C4	18p	18p	F
C5	68p	68p	F
C6	18p	15p	F
C7	18p	15p	F
C8	NC	NC	F
L1	180n	180n	H
L2	56n	33n	H
L3	27n	18n	H
L4	56n	56n	H
Y1	9.84375	13.560	Mhz
U1	CYF4455	CYF4455	



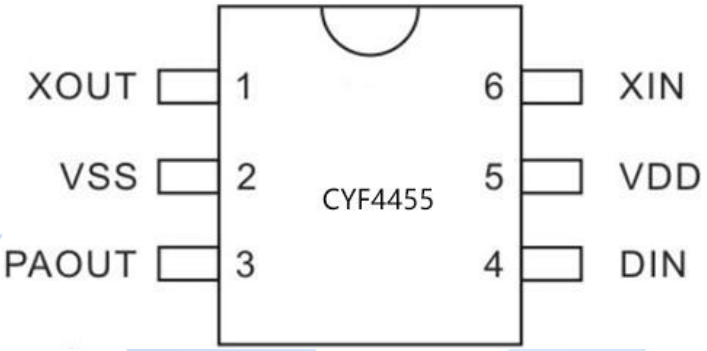
6. HARMONIC OUTPUT POWER:

Frequency	433.92M	867.84M	1301.76M	1735.68M	2169.6M	2603.52M	3037.44M	3471.36M	3905.28M	4339.2M
Output Power	9dbm	-45dbm	-32.2dbm	-40.5dbm	-62.3dbm	-61.26dbm	-73.25dbm	-74.47dbm	-80dbm	-78dbm

7. ORDER INFORMATION:

Valid Part Number	Package Type	Top Code
CYF4455	6 Pins, SOT23	CYF4455

8. PIN CONFIGURATION:



9. PIN DESCRIPTION:

Pin Name	I/O	Description	Pin No.
XOUT	O	Oscillator output	1
VSS	G	Ground connection	2
PAOUT	O	Power amplifier output	3
DIN	I	Data input	4
VDD	P	Power supply	5
XIN	I	Oscillator input	6

10. FUNCTION DESCRIPTION:

PA OUTPUT MATCHING

The PA output is an open-drain structure. Its output connects a large choke inductor to supply voltage and follows by a DC block capacitor. After the DC block capacitor, a C-L-C -type matching network is used to tune with the antenna impedance. The inductor and capacitor values may be different from the suggestion value depending on PCB material, PCB thickness, ground configuration, and the layout traces length.
For the open-drain structure in PA, the HBM (Human Body Mode) and MM (Machine Mode) ESD strength is 4KV and 400V.

REFERENCE OSCILLATOR:

For a quartz crystal to oscillate in the specified frequency, it should work with vendor provided load capacitor value, called CL. The load capacitor is about 12pF to 18pF in general. In CYF4455, the Pierce type crystal oscillator is used, and the shunt capacitor over XIN and XOUT is in series together equivalently. The shunt capacitor should be placed as 2x CL to oscillate with specified frequency. The temperature coefficient of quartz crystal will cause the VCO output frequency drift in high/low temperature range.

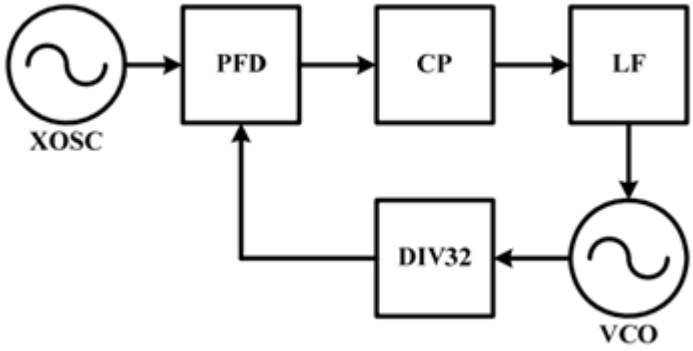
With a fixed divided-by-32 PLL, the fREFOSC= fTX / 32. The following table list fREFOSC for some common transmit frequencies.

Transmit Frequency f_{TX}	Reference Oscillator Frequency f_{REFOSC}
315 MHz	9.84375 MHz
340 MHz	10.625 MHz
390 MHz	12.188 MHz
433.92 MHz	13.56 MHz

PHASE-LOCKED LOOP (PLL):

The CYF4455 own a fixed divided-by-32 PLL to generate the transmitter signal. The PLL consists of the voltage-controlled oscillator (VCO), crystal oscillator, asynchronous ÷ 32 divider, charge pump, loop filter and phase-frequency detector (PFD). All these circuits are integrated on-chip. The PFD compares two signals and produces an error signal which is proportional to the difference between the input phases. The error signal passes through a loop filter with an

approximately 180 KHz bandwidth, and is used to control the VCO. A frequency divider placed after the VCO and it will feedback the divided signal to PFD. In the final the VCO will get locked to reference signal as fVCO = fREFOSC * 32. The block diagram below shows the basic elements of the PLL.



The PLL chain circuit is supplied by internal voltage regulator to ease the PA pulling and crystal spur issue.

ONE-SHOT CIRCUIT AND POWER-DOWN CONTROL:

During the signal transmission, the crystal oscillator start-up time will limit its wake-up time to work. A one-shoot circuit is used to solve this problem by turning on/off the power amplifier and PLL circuit separately.

When apply “HIGH” to DIN, will enable the PLL chain and PA. When applied“LOW” to DIN, the PA will be turn-off immediately, and the PLL chain will be turn-off after one-shot period about 50ms.

To calculate the re-triggerable one-shot delay time, it can be counted as 688128 / fREFOSC. For fREFOSC = 9.844MHz and 13.56MHz, the delay time is about 70ms and 50ms.

ANTENNA DESIGN AND PCB LAYOUT CONSIDERATION:

For a λ/4 dipole antenna and operating frequency, f (in MHz), the required antenna length, L (in cm), may be calculated by using the formula

$$L = \frac{7132}{f}$$

For example, if the frequency is 315 MHz, then the length of a λ/4 antenna is 22.6 cm. If the calculated antenna length is too long for the application, then it may be reduced to λ/8, λ/16, etc. without degrading the input return loss. Usually, when designing a λ/4 dipole antenna, it is better to use a single

conductive wire (diameter about 0.8 mm to 1.6 mm) rather than a multiple core wire.

If the antenna is printed on the PCB, ensure there is neither any component nor ground plane underneath the antenna on the backside of PCB. For an FR4 PCB (εr = 4.7) and a strip-width of 30 mil, the length of the antenna, L (in cm), is calculated by

$$L = \frac{c}{4 \times f \times \sqrt{\varepsilon_r}}$$

where “c” is the speed of light (3 x10^{10} cm/s

Proper PCB layout is extremely critical in achieving good RF performance. At the very least, using a two-layer PCB is strongly recommended, so that one layer may incorporate a continuous ground plane. A large number of via holes should connect the ground plane areas between the top and bottom layers.

Careful consideration must also be paid to the supply power and ground at the board level. The larger ground area plane should be placed as close as possible to all the VSS pins. Grounding the metal case of quartz crystal and isolate the XIN/XOUT trace to other can suppress the crystal spur signal over PA output.

11. ABSOLUTE MAXIMUM RATINGS：

(V_{SS}=0V)

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage Range	V_{DD}	-0.3	5	V
I/O Voltage	$V_{I/O}$	-0.3	5	V
Operating Temperature Range	T_A	-40	+85	°C
Storage Temperature Range	T_{STG}	-55	+125	°C

RECOMMENDED OPERATING CONDITIONS：

(V_{SS}=0V)

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage Range	V_{DD}	-0.3	3.6	V
Operating Temperature Range	T_A	-40	+85	°C

12. ELECTRICAL CHARACTERISTICS:

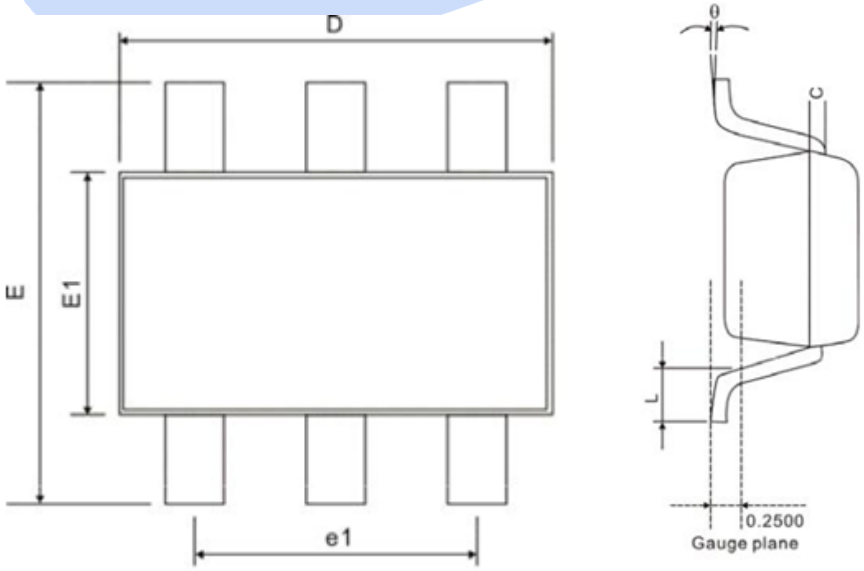
Nominal conditions: VDD = 3.0 V, VCC = 0 V, TA = +27°C.

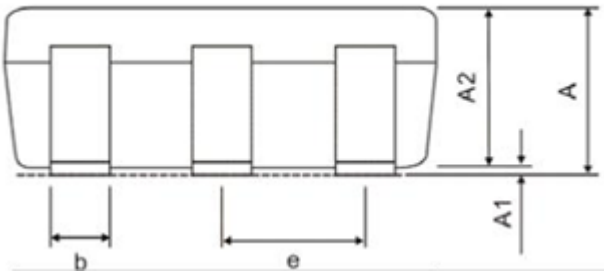
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
General Characteristics						
Supply Voltage	V_{DD}		2.2	3.0	3.6	V
Operating Current (Note)	I_{DD}	DIN=High(CW mode); P_{OUT} =14dBm, f_{RF} = 315MHz		12.5		mA
		DIN=High(CW mode); P_{OUT} =14dBm, f_{RF} = 434MHz		12.5		mA
Standby Current	$I_{standby}$	DIN=Low; T_{DELAY}>50ms			1	A
RF						
Frequency Range	f_{RF}		250		450	MHz
Power Amplifier Output Power (Note)	P_{out}	f_{RF} = 315MHz		14		dBm
		f_{RF} = 434MHz		14		dBm
RF Power On / Off Ratio	P_{EXT}			60		dB
Phase Noise	P_{NOISE}	315MHz, 10KHz offset		-75		dBc/Hz
Harmonics (Note)	P_{HARM}	2x/3x f_{RF}		-40		dBc
Crystal Spur	P_{SPUR}	f_{RF} = 315MHz		-50		dBc
		f_{RF} = 434MHz		-50		dBc
Data Input and One-shot						
Data Rate	D_{RATE}		0.5	2	20	Kbps
Crystal Oscillator Start-up Time	T_{ON}	C_L not connected		1		ms
One-shot Delay Time	T_{DELAY}		50			ms

Note: Depend on power amplifier output matching

13. PACKAGE INFORMATION:

6 Pins, SOT23-6





Symbol	Min.	Nom.	Max
A	-	-	1.45
A1	0.00	-	0.15
A2	0.90	1.15	1.30
b	0.30	-	0.50
c	0.080		0.200
D			
E			
E1			
e			
e1			
	0°		8°
L	0.30	0.45	0.60

Notes:
1. Refer to JEDEC MO-178
2. All dimensions are in millimeter

For more information and assistance, please contact us as follows:

CY WIRELESS TECHNOLOGY LIMITED
Add: 1407, Block C, Tairan Building, 8th Tairan Road, Futian District, Shenzhen, Guangdong Province, China
Website：www.rficy.com
Email: info@rficy.com